

This article was downloaded by: [University of California, San Diego]

On: 07 August 2012, At: 12:07

Publisher: Taylor & Francis

Informa Ltd Registered in England and Wales Registered Number: 1072954 Registered office: Mortimer House, 37-41 Mortimer Street, London W1T 3JH, UK



Molecular Crystals and Liquid Crystals

Publication details, including instructions for authors and subscription information:

<http://www.tandfonline.com/loi/gmcl20>

Fabrication of ZnO-Based Flexible Thin-Film Transistors by a Low-Temperature Process

Jin Woo Yang^a, Gun Woo Hyung^b, Ho Won Lee^a, Jae-Hoon Park^d,
Ja Ryong Koo^a, Kyung Seo Jung^c, Eou Sik Cho^c, Sang Jik Kwon^c &
Young Kwan Kim^a

^a Department of Information Display, Hongik University, Seoul, Korea

^b Department of Materials Science and Engineering, Hongik University, Seoul, Korea

^c Department of Electronics Engineering, Kyungwon University, Kyunggi-do, Korea

^d Department of Electrical, Information and Control Engineering, Hongik University, Seoul, Korea

Version of record first published: 18 Oct 2011

To cite this article: Jin Woo Yang, Gun Woo Hyung, Ho Won Lee, Jae-Hoon Park, Ja Ryong Koo, Kyung Seo Jung, Eou Sik Cho, Sang Jik Kwon & Young Kwan Kim (2011): Fabrication of ZnO-Based Flexible Thin-Film Transistors by a Low-Temperature Process, *Molecular Crystals and Liquid Crystals*, 550:1, 205-211

To link to this article: <http://dx.doi.org/10.1080/15421406.2011.599743>

PLEASE SCROLL DOWN FOR ARTICLE

Full terms and conditions of use: <http://www.tandfonline.com/page/terms-and-conditions>

This article may be used for research, teaching, and private study purposes. Any substantial or systematic reproduction, redistribution, reselling, loan, sub-licensing, systematic supply, or distribution in any form to anyone is expressly forbidden.

The publisher does not give any warranty express or implied or make any representation that the contents will be complete or accurate or up to date. The accuracy of any instructions, formulae, and drug doses should be independently verified with primary sources. The publisher shall not be liable for any loss, actions, claims, proceedings,

demand, or costs or damages whatsoever or howsoever caused arising directly or indirectly in connection with or arising out of the use of this material.

Fabrication of ZnO-Based Flexible Thin-Film Transistors by a Low-Temperature Process

JIN WOO YANG,¹ GUN WOO HYUNG,² HO WON LEE,¹
JAE-HOON PARK,⁴ JA RYONG KOO,¹ KYUNG SEO JUNG,³
EOU SIK CHO,³ SANG JIK KWON,³
AND YOUNG KWAN KIM^{1,*}

¹Department of Information Display, Hongik University,
Seoul, Korea

²Department of Materials Science and Engineering, Hongik University, Seoul,
Korea

³Department of Electronics Engineering,
Kyungwon University, Kyunggi-do, Korea

⁴Department of Electrical, Information and Control Engineering,
Hongik University, Seoul, Korea

In this paper we have studied a low-temperature process of fabricating zinc oxide (ZnO) thin-film transistors (TFTs) on polyethylene terephthalate (PET) substrate. PET film has a lower glass transition temperature ($T_g = 120^\circ\text{C}$) than costly Polyethersulphone (PES) film ($T_g = 230^\circ\text{C}$). Therefore we applied a low-temperature cross-linked polyvinylphenol (c-PVP) process to annealing at 110°C instead of the conventional c-PVP process (annealing at 165°C). The resulting TFTs based on oxide fabricated by the low-temperature process were similar in electrical characteristics to conventional TFTs. In addition, the ZnO TFTs fabricated by the low-temperature process exhibited a field-effect mobility of $0.075\text{ cm}^2/\text{Vs}$, a threshold voltage of 15 V and an on/off ratio of 1.7×10^5 respectively.

Keywords zinc oxide thin-film transistor; PET substrate; low-temperature process

Introduction

Oxide semiconductors have been extensively studied due to their excellent ambient stability and optical transparency [1–3]. In particular, oxide thin film transistors (TFTs) are expected to use switching devices within active matrix liquid crystal displays and organic light emitting diodes [4, 5]. There are a number of reports on TFTs that incorporate transparent materials such as zinc oxide (ZnO) as the active channel layer [7, 8]. However, the success of oxide semiconductors in the marketplace depends critically on the ability of these materials to sustain their electrical performance on a flexible substrate. The reason for this importance is that flexible electronics permits the development of displays that are thin, light, robust, conformable, and can, if required, be rolled away when not in use. In addition, the use of available low temperature process plastic-based substrates opens up the possibility of

*Corresponding author. E-mail: kimyk@wow.hongik.ac.kr

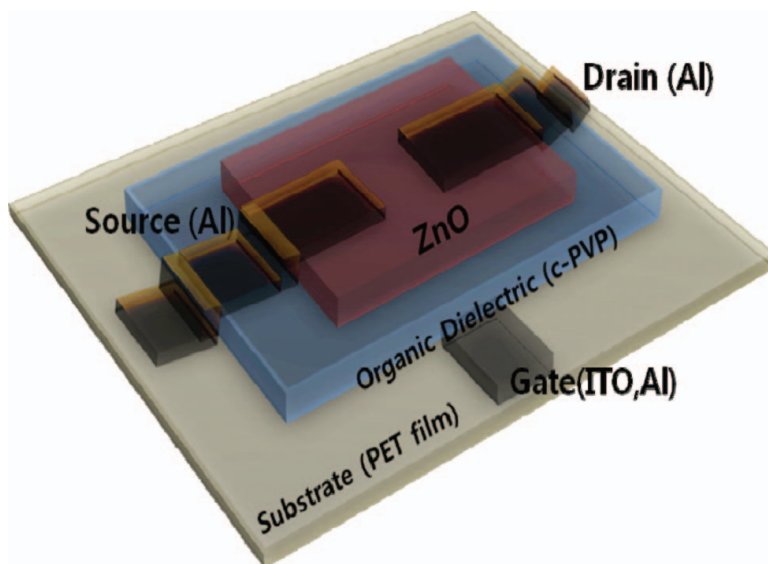


Figure 1. Structure of a bottom-contact low temperature process-based ZnO TFT fabricated on a transparent flexible PET substrate.

cost-effective processing in high volumes of roll to roll processing [9–11]. However, in the case of the R2R process, processing on low-priced PET film even with its low glass transition temperature can reduce their fabrication costs more effectively compared to using expensive PES film.

Therefore, in this work we studied the low-temperature fabrication process of zinc oxide (ZnO) thin-film transistors (TFTs) based on a polyethylene terephthalate (PET) substrate with an organic gate dielectric.

Experimental

TFTs based on oxide fabricated bottom-gate and top-contact structures are described in Fig. 1. To deposit on this structure, 180 nm thick indium-tin-oxide (ITO) as a gate electrode was deposited on PET substrate and patterned using conventional photolithography. An Al gate electrode was deposited by a thermal evaporator. As a gate dielectric layer, dissolved cross-linked poly-vinyl phenol (c-PVP) in 2-Propanol anhydrous (IPA) as an organic dielectric layer was formed using spin-coating on the gate electrode and then it was cross-linked by thermal baking at 110°C in a vacuum oven for a duration of 1 hour for the low-temperature process [12]. As an n-type semiconductor, ZnO films were deposited on the c-PVP as gate dielectric using zinc precursors diethylzinc (DEZn, $\text{Zn}(\text{C}_2\text{H}_5)_2$) and deionized water as an oxygen precursor. The ZnO films' rate of growth was defined to be about 6.8 Å/cycle, and the substrate was heated for 73 cycles at 120°C. Therefore, we studied one of the most important elements of fabrication in less than 120°C on the flexible PET substrate. The drain and source electrodes were deposited by the thermal evaporation method though a shadow mask to form a 50 nm thick Aluminum layer. The fabricated ZnO TFTs have a channel length of 60 μm and a width of 300 μm ($W/L = 5$). The electrical characteristics of ZnO TFTs were measured by a semiconductor analyzer unit

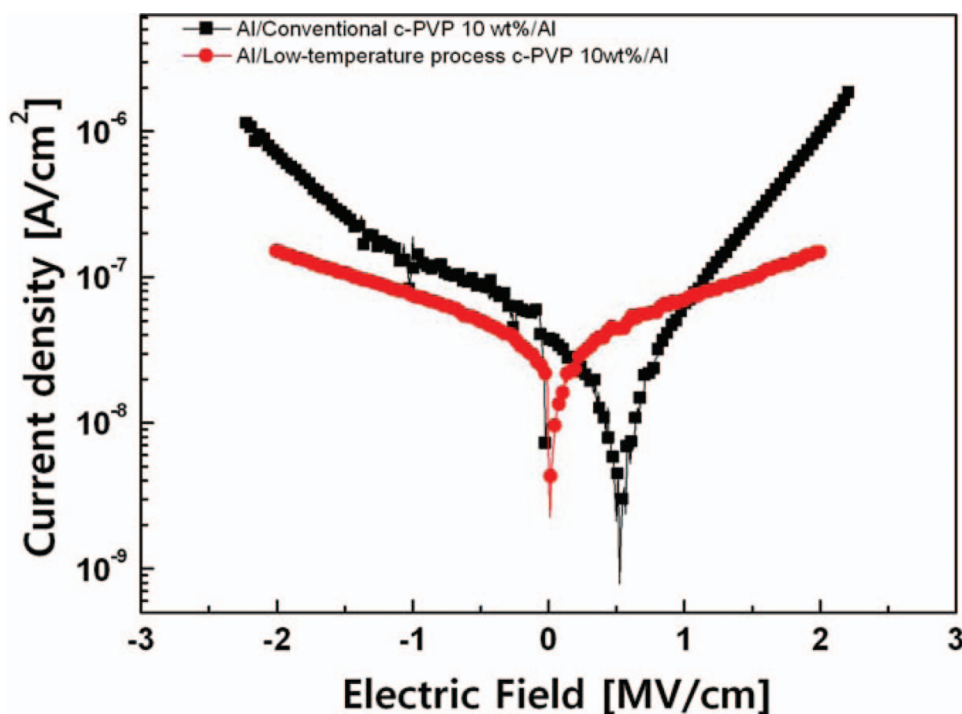


Figure 2. Current density–electric field (J–E) characteristics of MIM structures measured for different insulators: conventional c-PVP 10 wt%; and low-temperature process c-PVP 10 wt%.

(Keithley 4200-SCS). For investigating the lower processing temperature and fabrication on the low-priced plastic substrate, the current density–electric field (J–E) characteristics of the flexible MIM device were measured using an HP-4192 impedance analyzer.

Results and Discussion

In this paper we adapted the low-temperature process for ZnO TFTs on PET flexible substrates. Two types of devices were created according to the gate dielectric annealing environment and different gate dielectric layers for applying on the flexible substrate, respectively. The current density–electric field (J–E) characteristic curves of the MIM devices are represented in Fig. 2. Moreover, no electrical breakdowns were detected up to 2 MV/cm in the whole device. These results demonstrate that low-temperature process c-PVP is an also suitable gate insulator for flexible ZnO TFT applications. Figure 3 shows the capacitance–frequency (C–F) characteristics. The capacitance of the low-temperature process c-PVP 10 wt% gate insulator was 5.29 nF/cm² at 10 kHz. It shows a similar value to the conventional process c-PVP capacitance. The inset of Fig. 3 shows a contact angle image of the conventional c-PVP and low-temperature process c-PVP surface. This evidence suggests that the surface of the c-PVP layer and low-temperature process c-PVP layer show the approximate characteristics. Using Young's equation, the surface free energies of the gate dielectric layers were calculated to be about 39.8 mJ/m² for c-PVP and 36.5 mJ/m² for the low-temperature process c-PVP [13]. The optical transmittance spectra of bare glass, ITO/PET substrate and low-temperature c-PVP gate dielectric/ITO/PET substrate

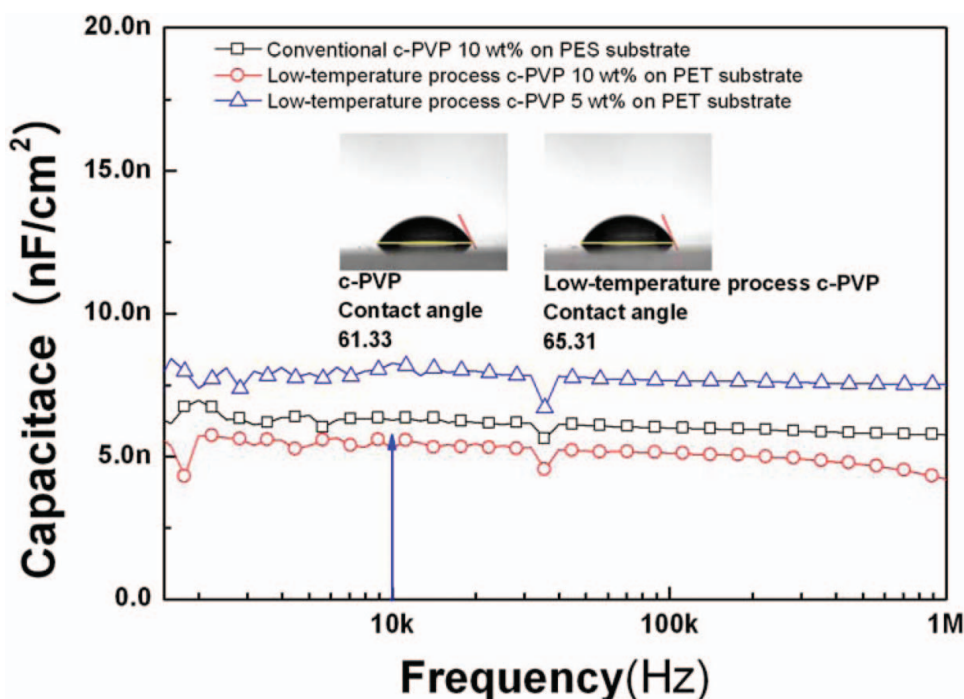


Figure 3. The capacitance - frequency (C-F) graph of TFTs using: a conventional c-PVP 10 wt% dielectric layer; a low-temperature process c-PVP 10 wt% dielectric layer; and a low-temperature process c-PVP 5 wt% dielectric layer. Inset shows the contact angle image of a conventional c-PVP and low-temperature process c-PVP surface.

are compared in Fig. 4. Except for the source and drain electrodes, the low-temperature c-PVP gate dielectric/ITO/PET substrate was highly transparent for the whole range of visible wavelengths with a transmittance as high as $\sim 90\%$ by glass standards, indicating that the spin-coated low-temperature c-PVP gate dielectric layer hardly affected the transmittance of the ITO/PET substrate. The inset of Fig. 4 is a top-view photograph of the ZnO TFTs, showing its clear visibility. Figure 5(a) shows the I_D-V_G curves of those figures, the on/off current ratio ($I_{on/off}$) and sub-threshold slope of ZnO-FETs, for the following three cases: using a conventional c-PVP 10 wt% on PES substrate; using a low temperature c-PVP 10 wt% on PET substrate; and using low temperature c-PVP 5 wt% on PET substrate. A comparison between the performance of conventional c-PVP 10 wt% and low-temperature c-PVP 10 wt% processing showed similar electrical characteristics. This indicates that the low temperature c-PVP process can be used instead of the conventional c-PVP process and still act as a good gate dielectric. Furthermore, we study the 5 wt% low temperature process c-PVP gate insulator for the improvement of field-effect mobility. By optimizing the concentration of insulator in the same voltage was able to induce more carriers. As a result, ZnO TFTs with low-temperature process c-PVP 5 wt% exhibited the typical n-type characteristics and good saturation behavior of the device to the same degree as the ZnO TFTs using conventional process c-PVP 10 wt%, as shown in Fig. 5. The mobility values of the low-temperature process c-PVP ZnO TFTs and the conventional process c-PVP ZnO TFTs were measured to be $0.075 \text{ cm}^2/\text{Vs}$ and $0.024 \text{ cm}^2/\text{Vs}$, respectively. Figure 5(b) shows the output characteristics I_{DS} versus V_{DS} of flexible ZnO TFTs. Table 1

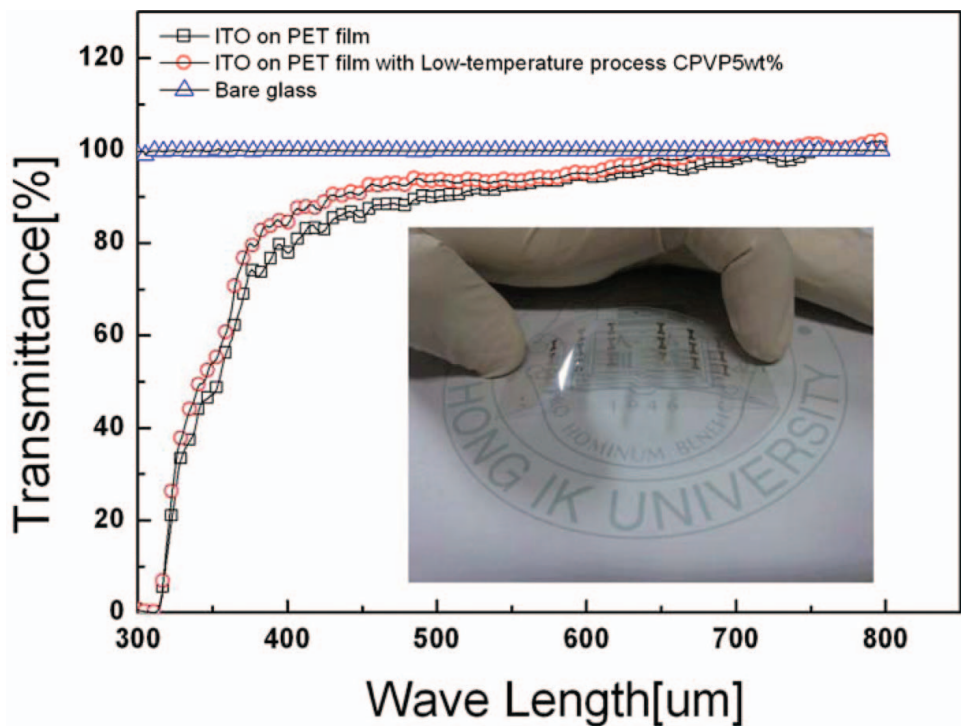


Figure 4. Comparison of the optical transmittance of bare glass, ITO/PET substrate and low-temperature c-PVP gate dielectric/ITO/PET substrate; inset is a top-view photograph of ZnO TFTs for clarity.

shows the summarized electrical properties for three kinds of ZnO TFTs. Using the low-temperature process c-PVP layer shows some improvement of the field effect mobility and high transmittances with the ITO gate electrode. Moreover, using the PET substrate can dramatically lower the fabrication cost needed for mass production.

Table 1. The electrical parameters of fabricated ZnO TFTs.

	Conventional c-PVP 10 wt% on PES sub.	Low-temperature process c-PVP 10 wt% on PET sub.	Low-temperature process c-PVP 5 wt% on PET sub.
Gate electrode	Al	Al	ITO
Threshold voltage [V]	10	8	15
Subthreshold slope [V/decade]	2	3.7	2.5
On/Off current ratio	6.65×10^4	9.03×10^3	1.70×10^5
Mobility [cm^2/Vs]	0.024	0.020	0.075

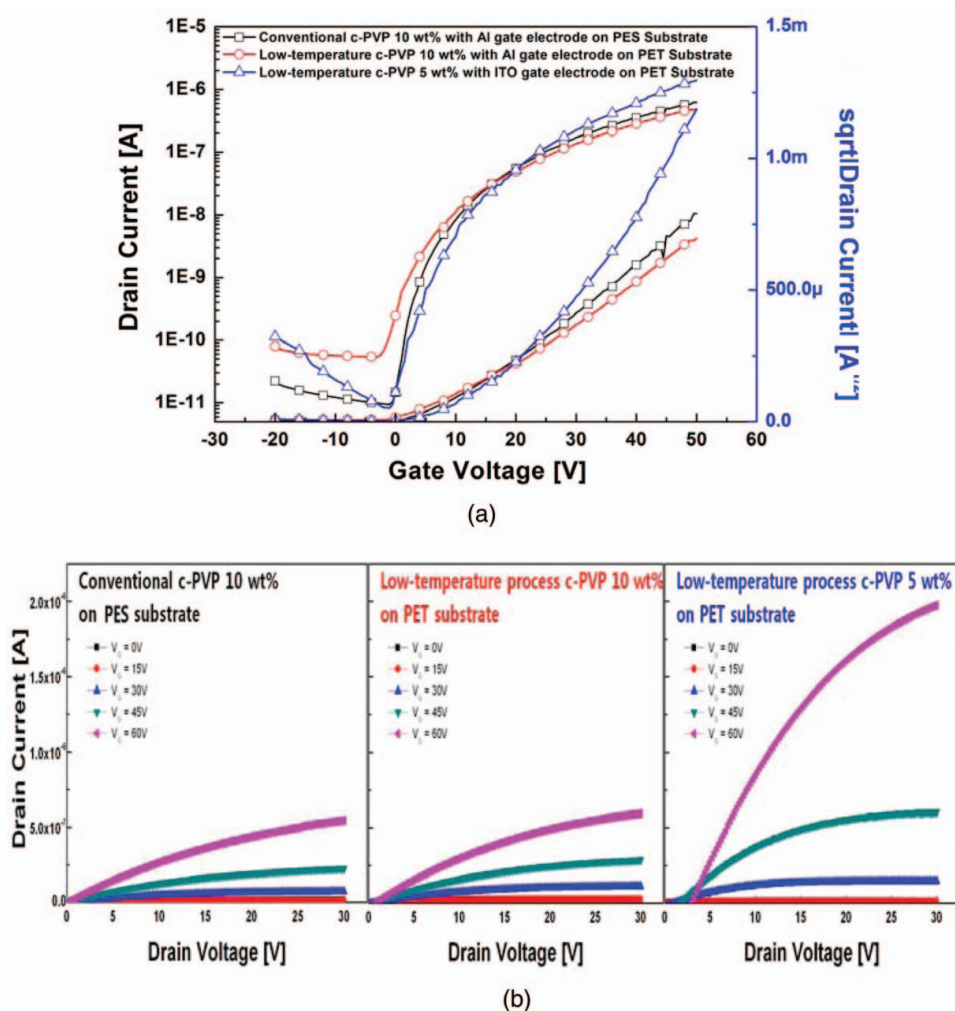


Figure 5. (a) Electrical characteristics of ZnO TFTs on a flexible substrate. The square root of the drain current $I_{DS}^{1/2}$ versus the gate voltage V_G , and I_{DS} versus V_G curves at the drain-source voltage of 30 V using an Al gate electrode and a conventional CPVP 10 wt% on PES substrate, using an Al gate electrode and a low temperature CPVP 10 wt% on PET substrate, and using an ITO electrode and a low temperature CPVP on PET substrate; (b) Output characteristics I_{DS} versus V_{DS} of flexible ZnO TFTs. Three types of devices were tested according to the gate dielectric annealing environment and different gate electrodes and flexible substrates.

Conclusions

In summary, we conclude that the low-temperature c-PVP process shows similar electrical characteristics in comparison with the conventional c-PVP gate dielectric process. In addition, ZnO TFTs using a low-temperature c-PVP layer and ITO gate electrode were shown to have high performance transmittance characteristics on the PET substrate. Therefore, an optimized process adapting the transparent gate electrode (ITO) and organic gate dielectric layer on a transparent flexible substrate will allow for the development of the all transparent

ZnO-FETs. Flexible ZnO-FETs on low-priced PET film might be an excellent candidate for transparent flexible devices in flexible flat panel displays or for other electronic applications.

Acknowledgment

This work was supported by the ERC program of the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea Ministry of Education, Science and Technology (MEST) (No. 20100009882).

References

- [1] R. L. Hoffman, B. J. Norris, and J. F. Wager, *Apply. Phys. Lett.*, **82**, 33 (2003).
- [2] P. F. Carcia, R. S. McLean, M. H. Reilly, and G. Nunes, Jr. *Apply. Phys. Lett.*, **82**, 1117 (2003).
- [3] E. Fortunato, P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira, and R. Martins, *Adv. Mater.*, **17**, 590, (2005).
- [4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, *Nature*, **432**, 488 (2004).
- [5] S. H. Cha, M. S. Oh, K. H. Lee, S. I. Im, B. H. Lee, and M. M. Sung, *Appl. Phys. Lett.*, **92**, 023506, (2008).
- [6] A. Bashir, P. H. Wöbkenberg, J. Smith, J. M. Ball, G. Adamopoulos, D. D. C. Bradley, and T. D. Anthopoulos, *Adv. Mater.*, **21**, 2226, (2009).
- [7] V. Srikant and D. R. Clarke, *J. Appl. Phys.*, **83**, 5447, (1998).
- [8] R. Navamathavan, C. K. Choi, E. J. Yang, J. H. Lim, D. K. Hwang, and S. J. Park, *Solid-State Electron.*, **52**, 813, (2008).
- [9] H. Yan, Z. H. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dotz, M. Kastler, and A. Facchetti, *Nature*, **457**, 679–U1, (2009).
- [10] H. Pan, Y. Li, Y. Wu, P. Liu, B. S. Ong, S. Zhu, and G. Xu, *J. Am. Chem. Soc.*, **129**, 4112 (2007).
- [11] J. B. Kim, C. Fuentes-Hernandez, S.-J. Kim, S. Choi, and B. Kippelen, *Org. Electron.*, **11**, 1074 (2010).
- [12] Y. G. Choi, H. J. Kim, K. S. Sim, K. C. Park, C. Im, and S.M. Pyo, *Org. Electron.*, **10**, 1209 (2009).
- [13] M. D. Duca and C. L. Plosceanu, *Poly Degrad.*, **61**, 65 (1998)